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What is Claimed Is
~~Claims:~~

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An apparatus for converting data between serial and parallel formats, comprising

at least one serial data channel (20),

a storage element (30) associated with each serial data channel (20) and having at least first and second arrays (31, 32) of storage cells (50, 50'), **characterised in that**

each storage cell comprises first and second ports, wherein the first ports of all storage cells (50, 50') of a storage element (30) are connected in parallel to a data bus (60) interconnecting the storage element (30) with the associated channel (20),

the data bus (60) comprises at least one buffering element (70) arranged to separate said data bus into portions (61-64), each portion being connected to the first port of at least one storage cell (50, 50') of each array (31, 32) of said storage element, and

means (100; 300) are provided for enabling the transfer of data between said bus (60) and at least one storage cell (50, 50') in said storage element (30) via said first port and enabling the transfer of data from one bus (61-64) portion to an adjacent bus portion via said at least one buffering element (70).

2. An apparatus as claimed in claim 1, **characterised in that** said means (100; 300) for enabling the transfer of data between said bus (60) and one storage cell (50, 50') comprises first clock generating means, said first clock being adapted to control access to said storage cell (50, 50')

and to control the transfer of data from one bus portion (61-64) to the next via said buffering element (70).

3. An apparatus as claimed in claim 2, **characterised in that** said first clock is adapted to the transmission speed of the associated serial data channel (20).

4. An apparatus as claimed in any preceding claim, **characterised in that** the first ports of the storage cells (50, 50') of each array (31, 32) are adapted to be accessed sequentially.

5. An apparatus as claimed in any preceding claim, **characterised in that** in each array, the first ports of storage cells (50, 50') disposed on each side of a buffering element (70) are adapted to be accessed simultaneously.

6. An apparatus as claimed in any preceding claim, **characterised in that** said buffering element (70) comprises a pipeline register.

7. An apparatus as claimed in any preceding claim, **characterised in that** the second ports of each storage cell (50, 50') are connected in parallel across all arrays.

8. An apparatus as claimed in any preceding claim, **characterised in that** means (200; 400) are provided for controlling the access to the storage cells (50, 50') of one array simultaneously via said second ports.

9. An apparatus as claimed in claim 8, **characterised in that** said means (200; 400) for controlling the access to the storage cells comprises a

second clock generating means.

10. An apparatus as claimed in any preceding claim, **characterised in that** said storage cells (50, 50') comprise dual-port random access memory (RAM) cells.

11. An apparatus as claimed in any preceding claim, **characterised in that** each array (31, 32) is dimensioned to store at least one data packet.

12. An apparatus as claimed in any one of claims 1 to 10, **characterised in that** each array (31, 32) is dimensioned to store part of a data packet.

13. An apparatus as claimed in any preceding claim, **characterised in that** said storage cells (50, 50') are arranged to store more than one bit simultaneously.

14. An apparatus for converting data from a serial to parallel format as claimed in any preceding claim, **characterised in that** said first port is a input port and said second port is an output port.

15. An apparatus for converting data from a parallel to serial format as claimed in any one of claims 1 to 12, **characterised in that** said first port is an output port and said second port is an input port.

16. An apparatus for converting data input through at least one channel in a serial format into a parallel format, comprising
at least one serial data input channel (20),
a storage element (30) associated with each serial data channel (20) and having at least first and second arrays (31, 32) of storage cells (50, 50'),

characterised in that

each storage cell (50, 50') comprises an input port and an output port, the input ports of the storage cells of the storage element (30) being connected in parallel to a data bus (60) interconnecting the storage element (30) with a serial channel (20),

said data bus (20) comprises at least one buffering element (70) arranged to separate said data bus into portions (61-64), each portion being connected to the input port of at least one storage cell (50, 50') of each array of said storage element, and

means (100) are provided for enabling the input of data from said data bus into at least one storage cell (50, 50') in said storage element (30) and enabling the buffering of data onto a data bus portion (61-64) by said at least one buffering element (70) in accordance with a predetermined input cycle.

17. An apparatus for converting data from a parallel format into a serial format, comprising

at least one serial data output channel (20),

a storage element (30) associated with each serial data channel (20) and having at least first and second arrays (31, 32) of storage cells (50, 50'),

characterised in that

each storage cell (50, 50') comprises an input port and an output port, the output ports of the storage cells (50, 50') of the storage element (30) being connected in parallel to a data bus (60) interconnecting the storage element with a serial output channel (20),

said data bus (60) comprises at least one buffering element (70) arranged to separate said data bus into portions (61-64), each portion being connected to the output port of at least one storage cell (50, 50')of each array of said storage element (30), and

means (300) are provided for enabling the output of data from at least one storage cell (50, 50') in said storage element (30) onto said data bus (60) and for enabling the buffering of data onto a data bus portion (61-64) by said at least one buffering element (70) in accordance with a predetermined output cycle.

18. A method for converting serial data to a parallel format utilising the apparatus as claimed in any one of claims 1 to 14 and 16, **characterised by** transmitting serial data from each channel (20) onto the associated data bus (60) and enabling the sequential input of data from the data bus (60) into the memory cells (50, 50') of one array (31, 32) of each storage element (30) in accordance with a write cycle.

19. A method as claimed in claim 18, **characterised by** enabling the simultaneous output of data from the memory cells (50, 50') of one array (31, 32) of each storage element (30) sequentially in accordance with a read cycle, the arrays (31, 32) in which data output and data input are enabled being different.

20. A method as claimed in claim 18, **characterised by** splitting the output of data from the memory cells (50, 50') of one array (31, 32) over at least two read cycles.

21. A method as claimed in any one of claims 18 to 20, **characterised by** enabling the transfer of data from one bus portion (61-64) to a following bus portion during each write cycle.

22. A method as claimed in claim 21, **characterised by** commencing the sequential input of data into each array (31, 32) from the portion of data

bus (64) arranged furthest from the associated serial data channel (20).

23. A method as claimed in claim 22, **characterised by** enabling the input of data to the storage cells (50, 50') at the end of one bus portion (61-64) and the beginning of the next bus portion simultaneously.

24. A method as claimed in any one of claims 18 to 23, **characterised by** adapting the write cycle for each storage element (30) to the transmission speed of the associated serial data channel (20).

25. A method as claimed in claim 24, **characterised by** adapting the read cycle to the total bandwidth of all serial data channels (20).

26. A method for converting parallel data to a serial format utilising the apparatus as claimed in any one of claims 1 to 13, 15 and 17, **characterised by**
enabling the sequential output of data from the memory cells (50, 50') of one array (31, 32) of each storage element (30) onto the data bus (60) in accordance with a read cycle and transmitting serial data from each data bus (60) onto the associated channel (20).

27. A method as claimed in claim 26, **characterised by** enabling the simultaneous input of data into the memory cells (50, 50') of one array (31, 32) of each storage element (30) sequentially in accordance with a write cycle, the arrays (31, 32) in which data output and data input are enabled being different.

28. A method as claimed in claim 26 or 27, **characterised by** splitting the input of data into the memory cells (50, 50') of one array (31, 32) over

at least two write cycles.

29. A method as claimed in any one of claims 26 to 28, **characterised by** enabling the transfer of data from one bus portion (61-64) to a following bus portion during each write cycle.

30. A method as claimed in claim 29, **characterised by** commencing the output of data from each array (31, 32) onto the portion of data bus arranged closest to the associated serial data channel (20).

31. A method as claimed in claim 30, **characterised by** enabling the output of data from the storage cells (50, 50') at the end of one bus portion (61-64) and the beginning of the next bus portion simultaneously.

32. A method as claimed in any one of claims 26 to 31, **characterised by** adapting the read cycle for each storage element (30) to the transmission speed of the associated serial data channel (20).

33. A method as claimed in claim 32, **characterised by** adapting the write cycle to the total bandwidth of all serial data channels (20).

34. A communications switch comprising an apparatus as claimed in any one of claims 1 to 17.

35. A communications switch as claimed in claim 34, **characterised in that** said apparatus operates in accordance with a method as claimed in any one of claims 18 to 33.